CLAIMS

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is as follows:

1. A method of forming an interconnect on a semiconductor substrate, comprising:

forming a relatively narrow first structure in a dielectric formed on a semiconductor substrate;

forming a relatively wider second structure in said dielectric formed on the semiconductor substrate;

forming a liner in said first and second structures such that said first structure is substantially filled and said second structure is substantially unfilled; and

forming a metallization over said liner to completely fill said second structure.

2. The method of claim 1, wherein said liner comprises one of a chemical vapor deposition (CVD) metal, a physical vapor deposition (PVD) metal and a plated liner.

3. The method of claim 1, wherein said liner comprises at least one of tungsten, aluminum, and titanium nitride.

4. The method of claim 1, wherein said metallization comprises copper.

5. A method of forming an interconnect on a semiconductor substrate, comprising:

forming a contact, including a slot, in a dielectric formed on a semiconductor substrate;

forming troughs into the dielectric, thereby to form a dual damascene structure;

depositing a conducting material on the dielectric;

depositing a metal over the conducting material to completely fill the slot and troughs;

removing the metal either to the conducting material or both the metal and the conducting material simultaneously back to the dielectric; and

selectively removing the conducting material.

6. The method of claim 5, wherein said dielectric comprises one of tetraethylorthosilicate (TEOS), silane and another low K polymer dielectric.

7. The method of claim 6, wherein said contacts comprise contacts formed between first and second metal levels formed on the semiconductor substrate.

8. The method of claim 5, wherein said conducting material comprises tungsten.

9. The method of claim 8, wherein the tungsten comprises chemical vapor-deposited (CVD) tungsten, a physical vapor deposition (PVD) tungsten, and a plated tungsten.

10. The method of claim 5, wherein a thickness of the conducting material is adjusted so as to completely fill the relatively small contacts.

11. The method of claim 5, wherein said metal comprises copper.

12. The method of claim 5, wherein the metal is removed by chemical mechanical polishing (CMP).

13. The method of claim 5, wherein said selectively removing comprises selectively removing said conductive material by a selective etch.

14. The method of claim 5, wherein said selectively removing comprises selectively removing said conductive material by a selective CMP.

15. The method of claim 5, further comprising:

depositing subsequent dielectric films and metal layers on the resulting structure.

16. A method of forming an interconnect on a semiconductor substrate, comprising:

forming troughs between first and second metal levels, including a slot, in a dielectric formed on a semiconductor substrate;

forming contacts in the dielectric, thereby to form a dual damascene structure;

depositing a conducting material on the dielectric;

depositing a metal over the conducting material to completely fill the slot and the troughs;

removing the metal either to the conducting material or both the metal and the conducting material simultaneously back to the dielectric; and

selectively removing the conducting material.

17. A semiconductor device, comprising:

a semiconductor substrate;

a dual damascene structure formed in at least one dielectric film formed on the semiconductor substrate, including a relatively narrow first structure and a relatively wider second structure;

a liner formed in said first and second structures such that said first structure is substantially filled and said second structure is substantially unfilled; and

a metallization formed over said liner to completely fill said second structure.

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